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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

1. (Currently Amended) An image display apparatus comprising:

a plurality of signal lines;

a plurality of display pixels arranged in a matrix to provide image display, each of said display pixels comprising a pixel electrode connected to said each of the plurality of signal lines via a pixel switch;

a plurality of data lines;

a plurality of memory cells for storing digital display data;

an image signal generating circuit for outputting an image signal to the signal lines based on said digital display data inputted from the plurality of memory cells via the data lines; and

wherein each of the plurality of memory cells comprises a memory switch connected to one of said data lines; a memory capacitor connected to said memory switch; and a field-effect transistor of which a source-drain path thereof is provided between a first node and a second node coupled to a corresponding one of said data lines,

wherein one electrode of said memory capacitor is connected to a gate of said field-effect transistor and another electrode of said memory capacitor is connected to said second node, and

wherein when a memory cell is read or written, a predetermined voltage is supplied to said first node.

2. (Original) An image display apparatus according to claim 1, wherein each of said plurality of display pixels is a liquid crystal display pixel having a counter electrode and a liquid crystal region between said pixel electrode and said counter electrode.

3. (Original) An image display apparatus according to claim 2, wherein said plurality of display pixels have an optical reflecting plate.

4. (Previously Presented) An image display apparatus according to claim 1, wherein said plurality of display pixels, said plurality of signal lines and said image signal generating circuit are formed on a single transparent substrate.

5-8. (Cancelled)

9. (Previously Presented) An image display apparatus according to claim 1, wherein said memory capacitor is a capacitor between a gate and a channel of said field-effect transistor.

10. (Previously Presented) An image display apparatus according to claim1, wherein said memory capacitor is a capacitor between a gate and a channel of a polycrystalline Si thin-film transistor (poly-Si TFT).

11-16. (Cancelled)

17. (Previously Presented) An image display apparatus according to claim 1, wherein some of said memory cells are connected to one data line, and said second node is connected to said corresponding data line through a selection switch.

18. (Cancelled)

19. (Previously Presented) An image display apparatus according to claim 17, wherein said selection switch is a polycrystalline Si thin-film transistor (poly-Si TFT) which is diode-connected in which the drain and the gate thereof are directly coupled.

20. (Original) An image display apparatus according to claim 17, wherein said selection switch is a p-n junction diode using a polycrystalline Si thin film.

21-22. (Cancelled)

23. (Previously Presented) An image display apparatus according to claim 17, wherein said memory cells are arranged in a matrix along said data lines extending in a y-direction, and said data lines are arranged by n line units in a case where unit digital display data composed of n bits is stored by n of said memory cells.

24. (Currently Amended) An image display apparatus according to claim 4, wherein lighting means to the display pixels is provided on a surface of said transparent substrate opposite to the surface on which the display pixels, the plurality of signal lines and the image signal generating circuit are arranged, and black matrix shielding is arranged between said transparent substrate corresponding to back portions of said memory ~~cells~~ cells and said lighting means.

25. (Cancelled)

26. (Previously Presented) An image display apparatus according to claim 1, wherein said image signal generating circuit has digital-to-analog converter for generating an image signal from display data stored in said memory cell.

27. (Previously Presented) An image display apparatus according to claim 2, wherein said image signal generating circuit has digital-to-analog converter for generating an image signal from said digital display data stored in said memory cell, and said digital-to-analog converter has a function of selectively outputting substantially two kinds of image signal voltages to the same digital display data.

28. (Previously Presented) An image display apparatus comprising:

a plurality of display pixels arranged in a matrix in order to provide image display, each display pixel comprising a pixel electrode and a pixel switch connected to said pixel electrode in series;

a digital-to-analog converter for outputting an image signal based on digital display data;

a group of signal lines for connecting said digital-to-analog converter to a group of pixel switches; and

display image selection means for writing said image signal in a given display pixel through said group of signal lines and said group of pixel switches, at least said plurality of display pixels, said group of signal lines and said digital-to-analog converter being formed on a single transparent substrate,

wherein said digital-to-analog converter contains a reference voltage generating circuit using a boron-doped polycrystalline Si (poly-Si) thin-film resistor as a gray scale voltage generating resistor.

29-39. (Cancelled)